Cyber Security Center

Université Bretagne Sud

Lab-STICC

Sciences and Technology
Laboratory of Information,
Communication and Knowledge

Cyrille CHAVET

Associate Professor
Embedded systems

“Doing science means accepting to be wrong a hundred times and to learn from one’s mistakes until the satisfaction of a good solution”

BIO

After exploring communications issues for the GAUT high-level tool as part of his thesis (2007 - UBS and STMicroelectronics-Grenoble), Cyrille Chavet spent a year at the TIMA laboratory in Grenoble before joining UBS in 2009 as associate professor. He is interested both in computer-aided design methodologies and in the optimization of communications within processors, more specifically in communication networks for flexible error-correcting code architectures. Currently, the FlexDEC-5G project immerses him in the issues related to 5G deployment. Work on the integration of constraints dealing with remote and low-speed communications will follow: updates of neural networks dedicated to AI, processor architectures intended for post-quantum encryption.

Link to full biography

50% of the researcher's activity devoted to cybersecurity

Focus :
Research [X]
Application field [X]

Core data

PhD students: 7

Post-doctoral fellows: 3

Publications: 6 - IEEE TSP, IEEE TCAD, IEEE TCAS-II, etc.

Conferences: 40 - DATE, FPL, ICCAD, ICASSP, ISCAS, GLS-VLSI, etc.

Book(s): 1 - Advanced Hardware Design for Error Correcting Codes, Springer 2015

Patent(s): 4 - Devices for communication; Hardware neural networks

International collaborations: University of Bologna (Italy)

Area(s) of research

CAD Tools and Hardware Security.

Fields of expertise

High Level CAD & Synthesis Tools.
Digital communications Architectures.
Post-quantum cryptography Architectures.

Applicative examples

Architecture optimization for error-correcting codes.
Securing digital communications.

Collaborative projects

FlexDEC-5G (FEDER / Leader: Turbo Concept) - development of 5G corrective code decoders.
SENSE (CominLabs project / Leader: LabSTICC) - neural networks with Telecom Bretagne, IRISA.
Project P (FUI / Leader: Airbus) - definition of a common model for the development of software and hardware systems with the Aerospace Valley, Systematic and industrial partners.

Domain

Communications & Hardware Security

Keywords

CAD & HLS
Hardware and software architecture
Digital communications
VDHL

Contact

cyrille.chavet@univ-ubs.fr
+33 2 97 87 45 67