Cyber Security Center
Université Bretagne Sud

Lab-STICC
Sciences and Technology
Laboratory of Information,
Communication and Knowledge

Philippe COUSSY

Full Professor
Embedded systems

“Research: a fantastic space of freedom”

BIO

A graduate of Paris 6 - Pierre and Marie Curie University, Philippe Coussy obtained his PhD on high-level synthesis at University Bretagne Sud in 2003. He appointed there as Associate Professor in 2004, obtained the ability to supervise research in 2011 and became full professor in 2014. His research activities focus on hardware architectures and associated software tools: high-level synthesis of non-programmable hardware accelerators, automatic generation of conflict-free memory interleavers, coarse-grained reconfigurable architectures and associated compilation tools, silicon neural network architectures, hardware and software design. Since 2015 he extended his field of research to the security of embedded systems. His research is supported by regional, national and international funding.

Link to full biography

Core data

25% of the researcher's activity devoted to cybersecurity

Focus :
Research [X]
Application field [X]

PhD students: 21

Post-doctoral fellows: 6

Publications: 15 - IEEE (TCAD, D&T, TNNLS, TSP), ACM (JETCS, TECS), etc.

Conferences: 70 - DATE, ASP-DAC, ICCAD, FPL, ISCAS, ICASSP, SIPS, etc.

Book(s): 2 - "High-Level Synthesis: From Algorithm to Digital Circuit", 2008 Springer ; "Advanced hardware design for error correcting codes", 2008 Springer. Associate editor IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), IEEE Signal Processing Letters (SPL)

Award(s): IEEE Senior Member, Member of the HiPEAC Network of Excellence

Patent(s): 6 - Interleaving method, neural network architecture method, fault tolerance device, active cache…

International collaborations: University of Bologna (Italy), ETH Zurich (Switzerland), Polytechnic University of Milan (Italy), University of California in Los Angeles (USA), University of California in San Diego (USA), McGill University (Canada), Brown University (USA), University of Palakkad (India)...

Area(s) of research

Hardware architectures and associated software tools

Fields of expertise

High-level synthesis - Electronic Design Automation (EDA)

Applicative examples

GAUT open-source high-level synthesis tool

Responsabilités

- Deputy director Lab-STICC (since June 2020)
- Deputy Director Phd School MathSTIC (2017-2020)
- Director of the STIC (which evolved to Complex Systems Engineering) Master's Degree (2015-2020)
- Head of the Communications, Architectures, Circuits and Systems (CACS) division of Lab-STICC (2016-2020)
- Member of the scientific committee of the LATERAL Thales / Lab-STICC joint laboratory (2018-)
- Elected member of the International Technical Committee IEEE Signal Processing Society, Design and Implementation of Signal Processing Systems (DISPS) (2011 to 2013, 2015 to 2021)
- Member of the evaluation committee National Research Agency (NRA) INS (2012-2014), NRA Micro-Nano CES 24 (2015-2017)
- Co-Leader of the Math-STIC disciplinary group of the SICMA PhD School (2016-2017)
- In charge of the theme « Embedded Software and Hardware Architectures « of the Research Group Soc-SIP (2011-2016)

Domain

Electronic components design method

Keywords

High-level synthesis
Reconfigurable coarse grain architectures and associated tools
Automatic generation of conflict-free memory interleavers
Silicon neural network architectures

Contact

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